Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUT1**
2. **IN1**
3. **OUT2**
4. **IN2**
5. **OUT3**
6. **IN3**
7. **GND**
8. **IN4**
9. **OUT4**
10. **IN5**
11. **OUT5**
12. **IN6**
13. **OUT6**
14. **VCC**

**9 8 7 6 5**

**10**

**11**

**4**

**3**

**12 13 14 1 2**

**SiS906**

**.065”**

**.065”**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .065” X .065” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .000” P/N: MMC74C906M**

**DG 10.1.2**

#### Rev B, 7/1